REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-3, 6 under 35 USC § 102 (b) as being anticipated by Peterson (U.S. Patent No. 4,498,128); and claims 9-11 and 14 under 35 USC § 103 (a) as being unpatentable over Rybicki (U.S. Patent No. 5,483,182) in view of Peterson (U.S. Patent No. 4,498,128). In addition, the Examiner rejected claims 4, 5, 7, 8, 12, 13, 15, and 16 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. These rejections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1 - 16.

2. Claims 4, 5, 7, 8, 12, 13, 15, and 16 have been rejected under 35 USC § 112, second paragraph. The applicant has amended these claims to overcome this rejection.

3. Claims 1-3, 6 have been rejected under 35 USC § 102 (b) as being anticipated by Peterson (U.S. Patent No. 4,498,128). In particular, the Examiner stated that

> Peterson et al. disclose the claimed invention a current limiting in a DC-to-DC converter (figure 1-2), limiting duty cycle of the DC-to-DC converter to the zero loading duty cycle plus the duty cycle loading offset (column 3, line 1-40), a maximum inductor current of the DC-to-DC converter (column 2, line 55-70). In regards to claim 3, (column 5, line 1-15).

The Applicant respectfully disagrees.

Claim 1 claims a method for current limiting in a DC-to-DC converter that includes determining a current loading duty cycle of the DC-to-DC converter; comparing the current loading duty cycle with a zero loading duty cycle of the output; and when the current loading duty cycle exceeds the zero loading duty cycle plus a duty cycle loading offset, limiting duty cycle of the DC-to-DC converter to the zero loading duty cycle plus the duty cycle loading offset.

In contrast, Peterson teaches that the primary current limit circuit operates in response to a peak current detected in a current sensing resistor 26. A current reaching a certain threshold biases the sensing transistor 25 into a conducting mode. Its collector is coupled to the duty cycle control circuit 24, which responds to reduce the overcurrent condition by limiting a duty cycle of the power switch 11. (Column 2, lines 54 - 63) Peterson teaches that the current limiting of Figure 2 functions in a similar manner. (Column 3, line 59 - Column 4, line 16)

As such, Peterson does not teach or suggest determining the duty cycle for a current loading condition as is presently claimed. Instead, Peterson teaches measuring current through a sense resistor. Further, Peterson does not teach or suggest comparing the current loading duty cycle with a zero loading duty cycle. Instead, Peterson teaches biasing a bi-polar transistor to conduct when a peak current through the sense resistor reaches the biasing level of the sensing transistor. Accordingly, Peterson does not anticipate claim 1.

Claims 2 and 3 are dependent upon claim 1, which has been shown to overcome the present rejection. Since each of claims 2 and 3 introduce additional patentable subject matter with respect to claim 1, the applicant believes that claims 2 and 3 overcome the present rejection.

Claim 6 claims a method for current limiting a DC-to-DC converter that includes monitoring duty cycle of the DC-to-DC converter to produce a monitored duty cycle; equating the monitored duty cycle to an inductor current based on a relationship between the inductor current and the duty cycle of the DC-to-DC converter to produce an equated current; comparing the equated current with a current limit threshold; and when the equated current compares unfavorably with the current limit threshold, limiting the inductor current based on the current limit threshold.

Peterson does not teach or suggest monitoring duty cycle of the DC-to-DC converter or equating the monitored duty cycle to an inductor current. Instead, Peterson teaches monitoring for a peak current through a sensing resistor. Accordingly, Peterson does not anticipate claim 1.

4. Claims 9-11 and 14 have been rejected under 35 USC § 103 (a) as being unpatentable over Rybicki (U.S. Patent No. 5,483,182) in view of Peterson (U.S. Patent No. 4,498,128). In particular, the Examiner stated:

Rybicki discloses the claimed invention an on-chip DC-to-DC converter (figure 2 and 3), an external inductor (figure 2, item 14), an output capacitance (figure 2, item 20); the regulation module provides current limiting of the output (figure 2, item signal 50), a comparator (figure 2, item 42). However Rybicki does not disclose the utilization technique for a limiting duty cycle of the output to the zero loading. Peterson et al. disclose the utilization of the similar technique for a limiting duty cycle of the output to the zero loading (column 3, line 1-40). It would have been obvious one having an ordinary skill in the art at the time the invention was made to modify Rybicki DC-DC converter by utilizing the technique taught by Peterson et al. for the purpose of increasing efficiency and reliability.

The applicant respectfully disagrees.

Claim 9 includes similar current limiting limitations as in claim 1. As such, regardless of whether Rybicki teaches an on-chip DC-DC converter, Peterson fails to teach or suggest the current limiting limitations of claim 9. Accordingly, a combination of Rybicki and Peterson fails to render claim 9 obvious.

Claims 10 and 11 are dependent upon claim 9, which has been shown to overcome the present rejection. Since each of claims 10 and 11 introduce additional patentable subject matter with respect to claim 9, the applicant believes that claims 10 and 11 overcome the present rejection.

Claim 14 includes similar current limiting limitations as in claim 6. As such, regardless of whether Rybicki teaches an on-chip DC-DC converter, Peterson fails to teach or suggest the current limiting limitations of claim 14.

Accordingly, a combination of Rybicki and Peterson fails to render claim 14 obvious.

For the foregoing reasons, the applicant believes that claims 1 - 16 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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